Abstract—This paper presents the design of the monolithic pseudo-differential buffer amplifier based on 0.25 um SiGe BiCMOS technology for mixer local oscillator (LO) input. LO buffer amplifier is implemented using pseudo-differential cascode circuit with voltage parallel feedback circuit. Buffer amplifier designed for 1.5-5 GHz frequency band and has power gain $G_T = 15$ dB with 0.5 dB ripple, 1-dB compression point $P_{1dB}$ is more than 15 dBm, chip size is 1.2×2.1 mm$^2$.

Index Terms—MMIC; SiGe; differential amplifier; buffer amplifier; local oscillator; cascode.

I. INTRODUCTION

The design of modern electronic circuits is a compromise between technical and economical performances. A broad frequency band allows expanding the range of possible applications of the designed circuits. A number of wireless protocols (mobile communications, wireless Internet, global navigation systems, etc.) works in the frequency band up to 5 GHz. Therefore, design of universal broadband electronic circuits that can overlap several frequency bands becomes actual.

Mixer is the key component that defines performance of the Mixer is the key component that defines performances of the many microwave systems. Passive double balanced mixer (DBM) offers excellent performances in terms of frequency band, port isolation, and intermodulation characteristics. The disadvantages of such mixers are negative conversion gain and high level of the required LO power [1]. One of the common way to overcome the latter problem is the using of the LO buffer amplifier (BA) [2]. This solution has an additional advantage of higher LO isolation from RF and IF ports.

Nowadays, modern SiGe technology offers the advantage of being low cost and having a high integration level. However, the main problems are poor RF output power and significant losses in transmission lines and elements. The major factor that limits the output power of the standard SiGe process is the transistor breakdown voltage. The combination of the common-base (CB) and common-emitter (CE) stage configuration, which is called “cascode”, provides the increasing of the breakdown voltage and output power, because the total DC voltage drop on each transistor [3–6]. Also, compared to the standard CE configuration, cascode has a higher power gain, low reverse transmission and low input capacitance.

In this paper, we report on the analysis, design and experimental investigation of a SiGe BiCMOS BA for the mixer LO input. The LO BA architecture has been designed using cascode topology with negative feedback circuit and a pseudo-differential structure. With proposed configuration BA has 1.5-4.5 GHz frequency band with 15 dB power gain $G_T$ and 1-dB compression point $P_{1dB}$ in one channel more than 15 dBm while consuming voltage and current were $V_{CC} = 5$ V and $I_C = 53$ mA. The chip is fabricated using the 0.25 um SiGe BiCMOS process (IHP, Germany). Die area of the LO BA is 1.2×2.1 mm$^2$ (including the pads).

II. STRUCTURE AND CIRCUIT DESIGN

A. Structure and requirements for LO BA

The overall structure of the mixer with LO BA is illustrated in the Fig. 1. The BA is located between balun and DBM to exclude the losses of LO power. It was decided to design the differential BA without baluns at the input and output ports because of more simple measurement interpretation and chip size economy.

![Fig. 1. Structure of the mixer with LO BA.](image-url)
to the mixer LO input impedance. It is reasonable to have a 2-3 dB margin in output power \( \text{Pout} \) to prevent nonlinear distortion of the LO signal. Besides, BA must be unconditionally stable in the whole frequency band.

**B. Cascode circuit**

One of the major factors that limits the output power of SiGe technology process is the transistor breakdown voltages. Because generally the high values of \( f_T \) and \( f_{MAX} \) (and power gain \( G_T \)) are obtained due to breakdown voltage sacrificing [7]. The used 0.25 µm SiGe BiCMOS technology offers three different types of the HBT NPN transistors: standard, high-performance and high-voltage. Despite the facts that high-voltage transistors have breakdown voltage \( V_{BR} > 7 \) V and high-performance transistors have higher \( f_T \approx 80 \) GHz, the standard NPN configuration was chosen as a compromise between power gain and output power density.

The breakdown voltage \( V_{BR} \) for standard NPN transistor is 4 V, which limits the bias voltage \( V_{CC} \) to the 2-2.5 V. The cascode, a combination of the CB and CE configurations, as shown in Fig. 2, allows higher supply voltage \( V_{CC} \) in the range of 4-5 V. Moreover, cascode is more unilateral, hence more unconditionally stable than CE device, also it has higher maximum achievable gain \( G_{MAX} \) that allows to design only one-stage amplifier to fulfill the requirements.

The usage of several transistors in parallel may lead to the stability problems at high frequencies [5]. The reason is the parasitic inductance, which appears when the parallel transistor are connected with common microstrip line. To prevent the possible unstability the series resistance \( R_{stab} \) (Fig. 2) can be introduced. The value of the resistance \( R_{stab} \) should be enough to compensate the influence of the parasitic inductance, as usual \( R_{stab} \) is about 3-10 Ω. Also, the values of bias resistors \( R_{bias1} \) and \( R_{bias2} \) were optimized for supply voltage \( V_{cc} = 5 \) V.

**C. Circuit design**

As usual, the differential structure in amplifiers increases the output voltage swing and reduces sensitivity to the parasitic effects of the bonding wires and packaging [8]. Unfortunately, the tail current source of the differential structure will affect the performance of the amplifier, such as gain and efficiency. Therefore, the pseudo-differential structure was chosen for designing the LO BA as presented in Fig. 3.

The input matching networks consist of parallel RC-circuits \( (R_1, C_2 \) and \( R_8, C_{13}) \) with DC blocking capacitors \( (C_{11}, C_{13}) \), that stabilize the BA introducing the losses at low frequencies, and parallel LC elements \( (L_1, L_4, C_1 \) and \( C_{14}) \), that match input of each amplifier to the 50 Ω. The resistors \( R_3, R_4 \) and \( R_7 \) are used for biasing the cascode.

The broadband cascode cell uses a negative voltage feedback through series RC-circuit to improve the stability and to obtain the flat gain in the desired frequency band. The output matching network consist of shunt inductances \( L_2 \) and \( L_3 \), that used as a power supply, and series DC blocking capacitors \( C_6 \) and \( C_9 \).

The models of the passive elements and microstrip lines provided by the foundry were used for the LO BA performance simulation, except the output inductances. The output
inductances ($L_2$ and $L_3$) were modeled by the EM simulator software such as Momentum from Keysight Technologies.

### III. MEASUREMENT RESULTS

The chip microphotograph of the cascode LO BA fabricated on the 0.25 um SiGe BiCMOS technology is shown in Fig. 4. The pseudo-differential LO BA chip occupies the area of 1.2×2.1 mm (2.52 mm²) including the pads.

![Fabricated pseudo-differential LO BA](image)

Fig. 4. Fabricated pseudo-differential LO BA.

The chip was measured on-wafer using GSGSG probes with pitch 150 um both at the input and at the output ports. Keysight PNA-X network analyzer was used to measure the mixed-mode 4-port $S$-parameters matrix [9] in the frequency range up to 10 GHz. The supply voltages of the LO BA were $V_{B1} = 4.1$ V and $V_{B2} = V_{CC} = 5$ V while total output current was $I_C = 101$ mA.

Fig. 5 compares with good agreement the simulated and measured differential $S$-parameters (the first quadrant of the mixed-mode 4-port $S$-matrix). The measured input return loss ($|S_{11}|$) is better than -10 dB from 1.5 to 5 GHz. Over this frequency range, output return loss ($|S_{22}|$) is better than -5.5 dB. The amplifier achieves power gain $G_T$ about 15.5 dB with ripple about 0.5 dB from 1 to 5 GHz.

The output matching of the LO BA is a compromise between delivered output power $P_{out}$, return losses and amplifier size. A little difference between measured and simulated output return loss $|S_{22}|$ and power gain $G_T$ can be caused by the EM modeled output inductances and nonlinear HBT models inaccuracy. Although it is not shown in the measurement results, reverse isolation ($|S_{12}|$) is better than -41 dB in the whole frequency range due to cascode features.

![Measured and simulated differential $S$-parameters of the pseudo-differential LO BA](image)

Fig. 5. Measured and simulated differential $S$-parameters of the pseudo-differential LO BA.

The measured and simulated Rollett’s stability factor $K$ is illustrated in Fig. 6. The $K$-factor is greater than 1 in the whole frequency band that means unconditionally stability. The difference between measured and simulated stability factors caused by the inaccuracy of the active and passive PDK models.

![Measured and simulated differential $S$-parameters of the pseudo-differential LO BA](image)

Fig. 6. Measured and simulated differential $S$-parameters of the pseudo-differential LO BA.

The variation of the power gain $G_T$ from bias current is shown in Fig. 7. As it could be seen, the impact of the collector current $I_C$ on the amplifier gain is not very high, mostly bias point will influence on the output power (Fig. 8).

![1-dB compression point](image)

The 1-dB compression point $P_{1dB}$ of the pseudo-differential LO BA was measured on-wafer using GSGSG probes, DC probes and Keysight PNA-X network analyzer. Due to differential structure of the LO BA and lack of broadband balun the $P_{1dB}$ measurement were performed only for half of the LO BA using the $In^+$ and $Out^+$ ports (Fig. 4). The rest two ports ($In^-$ and $Out^-$) were terminated by 50 Ω loads. However, due to the common bias circuits, the LO BA will consume as a full amplifier. So, one need to divide the total collector current $I_{C\_total}$ by 2, to get current in one channel $I_{C\_half}$.
Fig. 7. Measured and simulated differential S-parameters of the pseudo-differential LO BA.

Fig. 8 shows the measured $P_{1dB}$ power at different total collector currents ($I_{C\text{total}} = 70; 106; 132$ mA). While consuming $V_{CC} = 5$ V and $I_{C\text{total}} = 106$ mA ($I_{C\text{half}} = 53$ mA), the LO BA has maximum $P_{1dB}$ of 17 dBm at 2 GHz with PAE about 18%. From 1.5 to 5 GHz measured 1-dB compression point $P_{1dB}$ is not less than 15 dBm when $I_{C\text{total}} > 100$ mA. The lack of output power from 1 to 1.5 GHz is caused by the poor output matching. One of the possible way to solve this problem is using more complex matching network or matching to the complex input impedance of the mixer LO port.

Thus, these experimental results validate the modeling of the pseudo-differential LO BA and demonstrate the capability of the 0.25 um SiGe BiCMOS to achieve a broadband output power.

IV. CONCLUSION

Theoretical, simulated and experimental studies of the pseudo-differential LO BA based on SiGe BiCMOS technology have been presented in this paper. The BA will be used at mixer differential input LO port to decrease the required LO power. To achieve a higher output power and flat gain the LO BA architecture has been designed using cascode topology with negative voltage feedback circuit and the pseudo-differential structure.

Proposed configuration of the LO BA has 1.5–4.5 GHz frequency band with 15 dB power gain $G_T$ and 1-dB compression point $P_{1dB}$ more than 15 dBm in one channel while consuming voltage and current were $V_{CC} = 5$ V and $I_C = 53$ mA. The chip is fabricated using the 0.25 um SiGe BiCMOS process (IHP, Germany). The die area of the LO BA is 1.2×2.1 mm² including the pads.

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